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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,784	01/03/2004	Shyi-Ming Pan	04102-URS	1489
33804	7590	04/21/2005	EXAMINER	
SUPREME PATENT SERVICES				MONDT, JOHANNES P
POST OFFICE BOX 2339		ART UNIT		PAPER NUMBER
SARATOGA, CA 95070		2826		

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,784	PAN ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 03 January 2004.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-23 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-23 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 03 January 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>1/3/04</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This office action is in response to the filing on 1/3/04 of the application.

Information Disclosure Statement

The examiner has considered the items listed on the Information Disclosure Statement (IDS). A signed copy of substitute Form PTO-1449 is enclosed herewith.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the insulating layer formed on top of the first semiconductor layer (line 4 of claim 1) must be shown as a component of a final structure or the feature canceled from the claims (claims 1-10). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The Specification is objected to for the following two reasons:

- (a) A light-emitting device comprising an insulating layer located on top of the first semiconductor layer according to claim 1 is not disclosed anywhere in the Specification, including the Drawings, as a final structural component.
- (b) Separately claimed (in claim 1) and thus separately existing first semiconductor and n-type GaN compound layers are not disclosed, nor are they illustrated in any of the final structures.
- (c) Applicant does not disclose said insulating layer to be made of metal, alloy, or their combination, as claimed in claim 6 and claim 21, nor does the Specification disclose the selection from a group consisting of SiO₂, Si₃N₄, AlN, TiN, TiO₂ and a combination thereof as recited by claims 5 and 20.

A full disclosure of claim 1 should be included in the Specification or the claimed subject matter not disclosed should be removed from the claim language.

Claim Objections

2. **Claims 1-10** are objected to because of the following informalities: the wording "insulting" should be replaced by "insulating" (see line 5 of claim 1). Appropriate correction is required.

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3. **Claims 1-10** are objected to under 37 CFR 1.75(d) because the remainder of the Specification does not disclose the claimed subject matter. In particular:

(a) A light-emitting device comprising an insulating layer located on top of the first semiconductor layer according to claim 1 is not disclosed anywhere in the Specification, including the Drawings, as a final structural component: the insulator layer SiO₂ (element 3) in Figures 1 is removed in the first embodiment (see par. [0013]) and is on top of the substrate in the second and third embodiments (Figures 2 and 3).

(b) Separately claimed (in claim 1) and thus separately existing first semiconductor and n-type GaN compound layers are not disclosed, nor are they illustrated in any of the final structures.

4. **Claims 5, 6, 20 and 21** are additionally objected to under 37 CFR 1.75(d), because the remainder of the Specification does not disclose the claimed subject matter. In particular, the remainder of the Specification does not disclose the insulating layer to be selected from the group of materials recited in claims 5 and 20, nor does the remainder of the Specification disclose that the insulating layer is made of metal, alloy, or their combination as recited in claims 6 and 21.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claims 1-5 and 10** are rejected under 35 U.S.C. 102(b) as being anticipated by Lester (6,091,085). Lester teaches (title, abstract, col. 2, l. 53 – col. 5, l. 63 and Figure 7) a light-emitting device (LED), comprising: a sapphire (claim 2 is met) substrate 33 (col. 5, l. 33 and col. 2, l. 56-57); a first semiconductor layer (n-GaN based layer within p-n GaN based junction 32 corresponding to 13 in Figure 1; col. 2, l. 53-59 and col. 5, l. 32-33; said first semiconductor layer, being n-GaN based, is n-type and thus claim 3 is met, while, with x=0 and y=0 claim 4 is seen to be met) formed on top of the substrate; an insulating layer 35 (col. 5, l. 34-47, comprising SiO₂, (see col. 5, l. 44-47) and thus claim 5 is met) formed on top of said first semiconductor layer; a mesa formed on the insulating layer and exposing the surface of the first semiconductor layer (the protruding portion of said first semiconductor layer 32 being fully analogous to mesa 4 of Applicant); and an LED structure (the complement of said n-GaN based layer within 32, i.e., the remaining portion of 32) formed on the exposed surface of the first semiconductor layer; where the LED being a light-emitting active layer 18 (being a p-n junction, claim 10 is met) and a p-type GaN II-V group compound layer (the inherently present light-emitting, i.e., active layer constituting the interface layer between the n-GaN based and p-GaN based layers of 32), the p-type GaN III-V group compound layer being connected to a p-type low-resistance ohm contact 34 (col. 5, l. 32-34) and an n-type GaN III-V group compound layer being connected to an n-type low-resistance ohm contact (on the right corresponding to element 16 (col. 3, l. 5-10)) to provide forward bias. In conclusion Lester clearly anticipates claim 1.

On claims 7, 9, 15 and 16: the further limitations as defined by claims 7, claim 9, claim 15 or claim 16 do not further limit the LED device but instead only limit its method of manufacturing. Applicant is reminded in reference to the claim language referring to "is fabricated with an e-gun, sputter or CVD method" intended use and other types of functional language including those pertaining exclusively to a method of making must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey, 152, USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

7. **Claims 11-13, 18, 19, 20 and 23** are rejected under 35 U.S.C. 102(b) as being anticipated by Lester (6,091,085). Lester teaches (title, abstract, col. 2, l. 53 – col. 5, l. 63 and Figure 7) a light-emitting device (LED), comprising: a sapphire (claim 12 is met) substrate 33 (col. 5, l. 33 and col. 2, l. 56-57); a first semiconductor layer (n-GaN based layer within p-n GaN based junction 32 corresponding to 13 in Figure 1; col. 2, l. 53-59 and col. 5, l. 32-33, while, with x=0 and y=0 claim 13 is met) formed on top of the substrate; a plurality of rectangular (cf. Figure 7: claim 19 is met) trenches 35 (col. 5, l. 34) formed in a part of (an) area of the first semiconductor layer and having a range for their depth (depth at least equal to half the distance between the top GaN surface and the sapphire substrate) that includes the range (depth > n-GaN thickness) as claimed (claim 18); an insulating layer 35 (cf. col. 5, l. 42-47) of SiO₂ (cf. col. 5, l. 47; hence claim 20 is met) formed in the trenches, said trenches having a depth greater than the thickness ; and an LED structure (the complement of said n-GaN based layer within 32,

i.e., the remaining portion of 32) formed on the exposed surface of the first semiconductor layer; where the LED being a light-emitting active layer 18 (being a p-n junction, thus meeting claim 23) and a p-type GaN II-V group compound layer (the inherently present light-emitting, i.e., active layer constituting the interface layer between the n-GaN based and p-GaN based layers of 32), the p-type GaN III-V group compound layer being connected to a p-type low-resistance ohm contact 34 (col. 5, l. 32-34) and an n-type GaN III-V group compound layer being connected to an n-type low-resistance ohm contact (on the right corresponding to element 16 (col. 3, l. 5-10)) to provide forward bias. In conclusion Lester clearly anticipates claim 11.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. ***Claims 8 and 22*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lester (6,091,085) in view of Imai et al (5,602,418). As detailed above, Lester anticipates claim 1 and claim 11. Lester does not necessarily teach the further limitation defined by claim 8 nor the further limitation as defined by claim 22, but Lester does teach the thickness of said insulating layer to be at least as large as half the distance between the top surface surface of the GaN based layer 32 and the sapphire substrate, i.e., half of the thickness of the LED structure. As evidenced by Imai et al a typical

thickness of said LED structure in the case of a GaN-based LED structure based on a p-n junction with thickness less than 3 μm (col. 10, l. 28-40), which substantially overlaps with the ranges as claimed in both claim 8 and claim 22. A *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. *In re Peterson*, 65 USPQ2d 1379 (CA FC 2003).

10. **Claims 6 and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lester (6,091,085). Although Lester does not necessarily teach the insulating layer 35 in his embodiment of Figure 7 to be made of metal, alloy or their combination (sic: an alloy combined with a metal is an alloy) it would have been obvious to substitute Al_2O_3 (sapphire) for SiO_2 in view of his first embodiment, in which the same function is performed by roughening the sapphire substrate by which sapphire protrusions 118 are created, while, furthermore, Lester teaches a general criterion (col. 5, l. 50) for the optimum material not satisfied less by Al_2O_3 than by SiO_2 , considering their respective refractive indices in the blue range (relevant for the blue light-emitter) are approximately 2 and 1.46, respectively (see Tropf et al, "Aluminum Oxide (Al_2O_3) Revisited", in "Handbook of Optical Constants of Solids", Ed. Edward D. Palik, page 653-660 on sapphire and M.S. Sze, "Modern Semiconductor Device Physics", Appendix J on page 545 on SiO_2). The selection of either can be viewed obvious over the other, in light of said criterion and in light of the use of both materials for the same purpose in different embodiments taught by Lester. Applicant is reminded in this regard that it has been held

that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. *In re Leshin* 125 USPQ 416.

11. **Claims 14 and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lester (6,091,085) in view of Yamasaki et al (6,670,647 B1). As detailed above, Lester anticipates claim 11. Lester does not necessarily teach the further limitation that the first semiconductor layer to have a thickness greater than 0.1 μm (claim 14). However, it would have been obvious to include said further limitation in view of Yamasaki et al, who, in a GaN based semiconductor light-emitting device teach the n-type GaN providing contact with the n-electrode (title, abstract, col. 5, l. 8 – col. 6, l. 20), hence directly corresponding to said first semiconductor layer in analogous art, teach the thickness of said n-GaN to be about 4 μm , which significantly overlaps with the claimed range for said thickness. A *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. *In re Peterson*, 65 USPQ2d 1379 (CA FC 2003).

Furthermore, *with regard to claim 17*, although Lester does not necessarily teach the further limitation as defined by claim 17, Lester does teach the range of the depth, say D, of the trenches on the first semiconductor layer to be determined by the range D $\geq (t_1+t_2)/2$, where t₁ and t₂ are the thickness of the first semiconductor layer (t₁) augmented with the thickness of the p-contact layer over it (t₂), while the p-contact layer

is usually much thinner than the n-contact layer, as evidenced by Yamasaki et al, who cites a thickness t₂ of about 0.5 μm (col. 6, l. 1-20). Therefore, the range of the prior art substantially overlaps the range claimed, D < t₁. *Motivation* to include said teaching by Yamasaki et al derives from the reduced light absorption for thinner p-GaN layers. A *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. *In re Peterson*, 65 USPQ2d 1379 (CA FC 2003).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Thibeault et al (6,657,236 B1), Thibeault et al (6,410,942 B2), Thibeault et al (6,821,804 B2) and Thibeault et al (US 2004/0041164 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
April 16, 2005

Patent Examiner:



Johannes Mondt (Art Unit: 2826)